Transistors, Amplifiers & Oscillators

Electronics study notes · FETs, BJTs, biasing, amplifier stages, switching, power amplifiers and feedback

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ABOUT AP DESIGN LABS

AP Design Labs is an Adelaide-based engineering studio specialising in bespoke, purpose-built technology for industries where off-the-shelf products simply don't cut it — farmers, vignerons, solar operators and EV charging. Every product is designed, prototyped and manufactured in-house, built to work reliably and independently, without subscription lock-in.

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Welcome

Welcome from AP Design Labs

I'm Andrew from AP Design Labs. If you've got a Pico or an ESP32 and a 3D printer, you know the drill: code from one site, wiring from another, no case, and it never quite works. My packs give you all of it in one place, tested and in MicroPython, for projects you'll actually use, like a lamp that glows green when SA power is cheap or a beacon that tells you it's bin night. You build it, print it, and it lives on your bench, not in a drawer.

Alongside the packs, I'm building a series of resource texts like this one, so makers can quickly find out how a component works and what it does, without digging through forums and datasheets. Each one pulls the essentials together in one place: clear diagrams, the key formulas and worked examples you can check your own circuits against.

This first text covers transistors, amplifiers and oscillators: the theory behind every sensor front-end, driver stage and switching circuit in an AP Design Labs build.

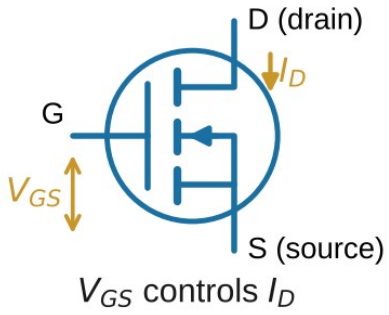
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1. Field-Effect Transistors

1.1 What is a FET?

- A FET is a **three-terminal** semiconductor device: gate (G), drain (D) and source (S).
- Drain current I_D is controlled by the **electric field** produced by the gate voltage.
- It is a **voltage-controlled, unipolar** device with very high input impedance.



Main features

- Majority-carrier operation
- High input impedance
- Low noise
- Low power consumption
- Good thermal stability

Common applications

- Amplifiers and buffers (voltage follower)
- Analog switches
- Voltage-controlled resistors
- CMOS and digital logic

> **Remember**
> **BJT** is current-controlled.
> **FET** is voltage-controlled.

1.2 The FET family

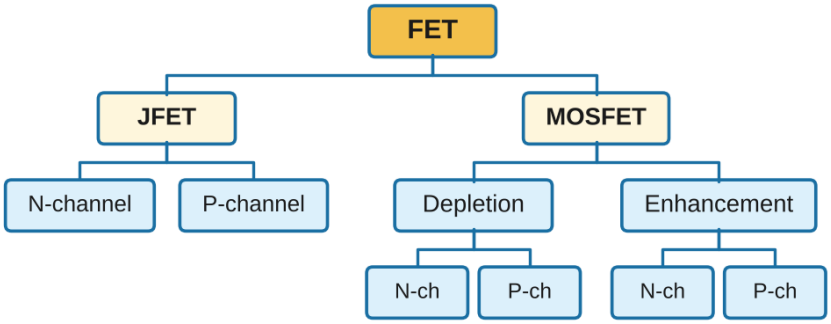


Figure 1 — The FET family: JFETs and MOSFETs, each in N- and P-channel forms.

2. JFET Construction & Working

2.1 Construction and circuit symbols

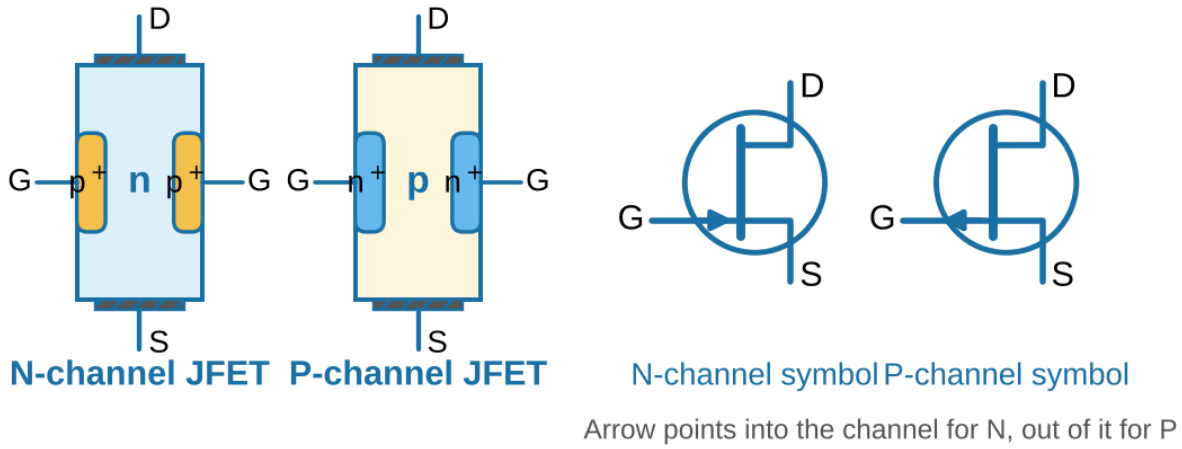


Figure 2 — JFET construction and symbols. The arrow points into the channel for N-channel, out of it for P-channel.

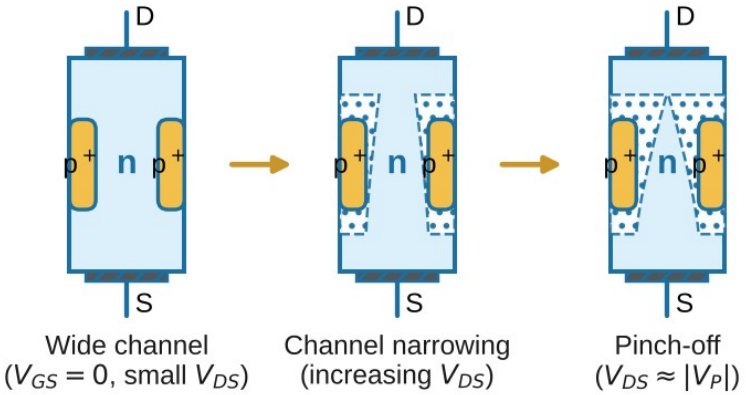
2.2 Working of an N-channel JFET

1. **V_{GS} = 0, small V_{DS}** — the channel offers low resistance and current I_D flows through it from drain to source.
2. **Increasing V_{DS}** — the depletion regions near the drain widen, so the channel narrows towards the drain end.
3. **At $V_{DS} \approx |V_P|$** — the depletion regions just meet at the drain end. The channel is pinched off and the current saturates.
4. **Beyond pinch-off** — I_D stays nearly constant (equal to I_{DSS} when V_{GS} = 0) in the saturation region until breakdown at a very high V_{DS}.

Effect of gate voltage

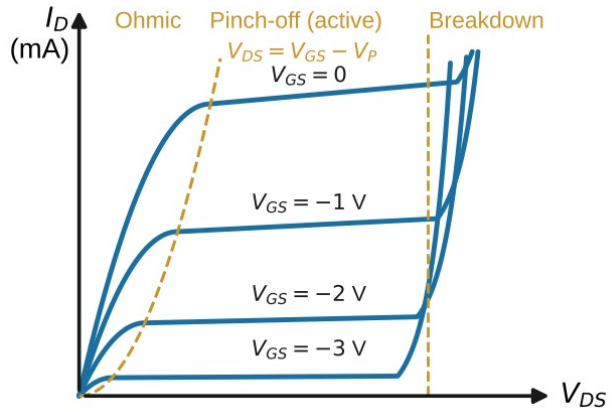
- For an N-channel JFET, V_{GS} is **negative** with respect to the source.
- A more negative V_{GS} widens the depletion regions, narrows the channel and reduces I_D.
- At $V_{GS} = V_{GS(off)} = -|V_P|$ the channel is completely cut off and $I_D \approx 0$.

Channel condition (N-channel)



3. JFET Characteristics

Drain characteristics



Transfer characteristic

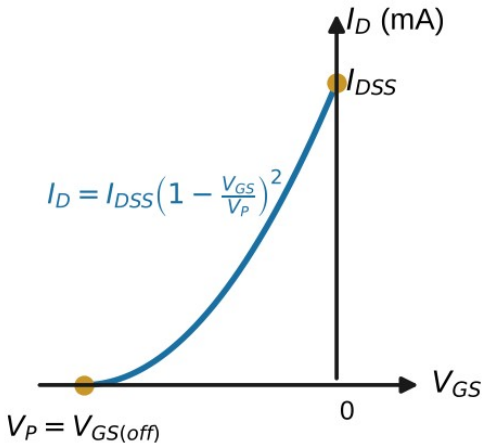


Figure 3 — Drain characteristics (ohmic, pinch-off and breakdown regions) and the transfer characteristic.

3.1 Shockley equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_P \le V_{GS} \le 0$$

I_D = drain current (A)

I_{DSS} = drain current at $V_{GS} = 0$ (the maximum drain current)

V_P = pinch-off voltage $V_{GS(off)}$; negative for an N-channel JFET

V_{GS} = gate-to-source voltage (V)

3.2 Important parameters

Transconductance g_m (S or mS)

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_{m0} = \frac{2 I_{DSS}}{|V_P|}$$

g_{m0} is g_m at $V_{GS} = 0$

Drain resistance r_d (Ω or kΩ)

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

Amplification factor μ (dimensionless)

$$\mu = g_m r_d$$

3.3 Worked example

Given: $I_{DSS} = 12$ mA, $V_P = -6$ V, $V_{GS} = -2$ V. **Find:** I_D

$$I_D = 12\left(1 - \frac{-2}{-6}\right)^2 = 12\left(\frac{2}{3}\right)^2 = 12 \times \frac{4}{9} = 5.33\,mA$$

4. FET Biasing & Comparison

4.1 BJT vs JFET vs MOSFET

Parameter	BJT	JFET	MOSFET
Control	Current-controlled	Voltage-controlled	Voltage-controlled
Carriers	Bipolar (electrons and holes)	Unipolar (majority carriers)	Unipolar (majority carriers)
Input impedance	Low to medium	High	Very high
Noise	Moderate	Low	Low
Typical use	High-gain stages	Low-noise input stages	Switching and CMOS

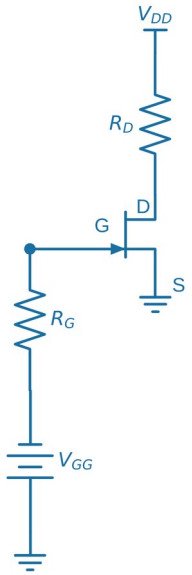
Table 1 — BJT, JFET and MOSFET compared.

> **Key point**
> FET gate current is ideally almost zero.

4.2 Why bias?

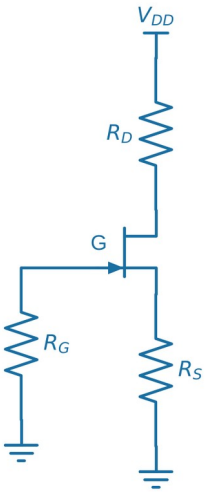
Biasing fixes a **stable Q-point** in the active region so the device can amplify without distortion. Three common JFET bias arrangements are shown below.

Fixed bias



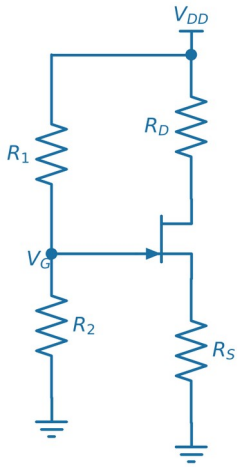
$$V_{GS} = -V_{GG}$$

Self bias



$$V_{GS} = -I_D R_S$$

Voltage-divider bias



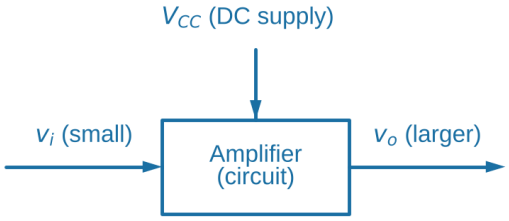
$$V_G = V_{DD}\frac{R_2}{R_1 + R_2}$$
$$V_{GS} = V_G - I_D R_S$$

The Q-point is the intersection of the bias line (above) with the Shockley curve, $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$.

5. Small-Signal Amplifiers

5.1 Purpose

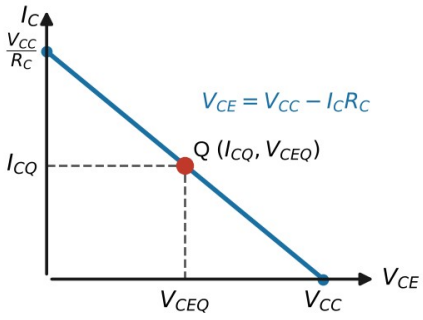
- An amplifier uses DC supply power to produce a **larger replica** of a small AC input signal.
- Proper biasing places the device at a **Q-point** so the output can swing without distortion.

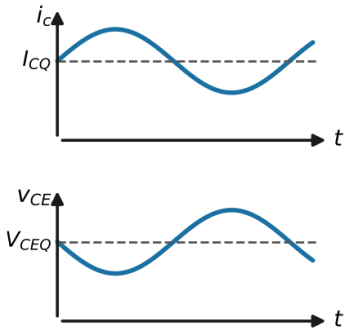


5.2 Important gains

Voltage gain	Current gain	Power gain	Voltage gain in decibels
$A_v = \frac{v_o}{v_i}$	$A_i = \frac{i_o}{i_i}$	$A_p = \frac{P_o}{P_i} \approx A_v A_i$	$A_{v(dB)} = 20 \log_{10} \lvert A_v \rvert$

5.3 DC load line and Q-point

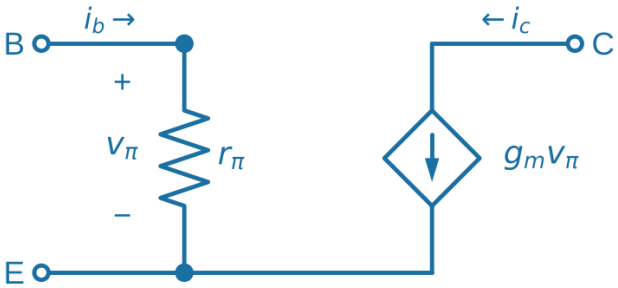




i_c and v_{CE} are 180° out of phase

- The load line $V_{CE} = V_{CC} - I_C R_C$ runs from $I_C = V_{CC}/R_C$ (saturation) to $V_{CE} = V_{CC}$ (cut-off).
- Biasing at the middle of the line gives a **symmetrical swing**.
- i_c and v_{CE} are **180° out of phase**.

5.4 Small-signal BJT model (hybrid-π)



$$g_m = \frac{I_C}{V_T}$$

$$r_\pi = \frac{\beta}{g_m}$$

$$V_T \approx 25\,mV$$

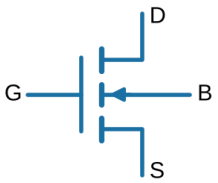
V_T at room temperature

A good amplifier needs
Sufficient gain · suitable input and output impedance · wide bandwidth · low distortion.

6. MOSFET Fundamentals

6.1 What is a MOSFET?

A **Metal-Oxide-Semiconductor FET** has an insulated gate separated from the channel by a thin layer of SiO_2, giving extremely high input impedance. The fourth terminal is the body (substrate), usually tied to the source.



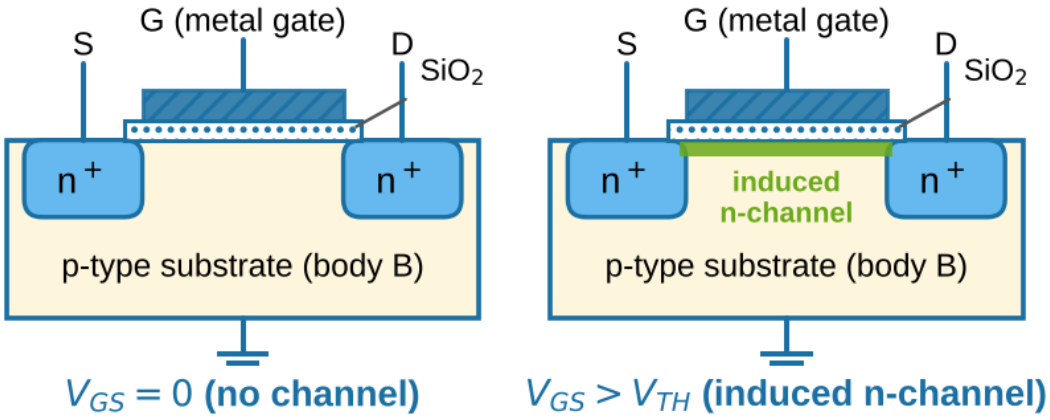


Figure 4 — Enhancement NMOS: no channel at $V_{GS} = 0$; an n-channel is induced when $V_{GS} > V_{TH}$.

6.2 Types of MOSFET

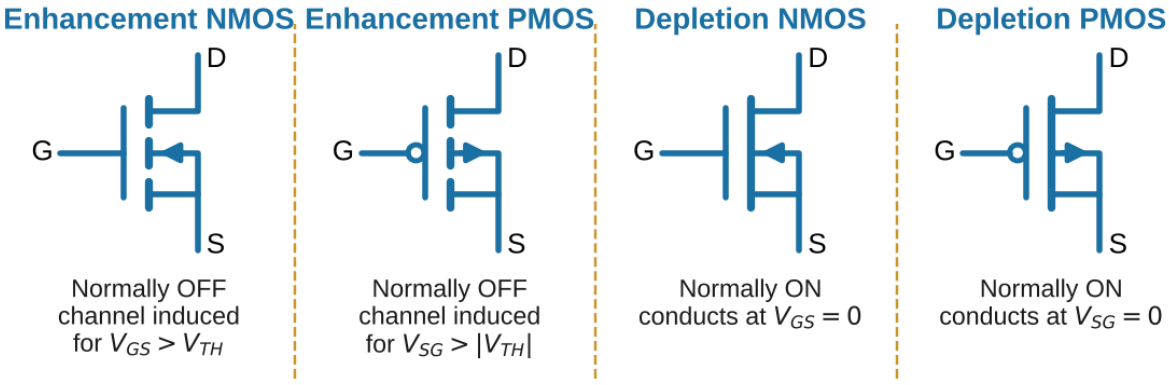


Figure 5 — Enhancement devices are normally OFF; depletion devices are normally ON.

6.3 Operating regions — enhancement NMOS

Region	Condition	Drain current I_D
Cut-off	$V_{GS} < V_{TH}$	$I_D \approx 0$
Triode (linear)	$V_{GS} > V_{TH}$ and $0 \le V_{DS} < V_{GS} - V_{TH}$	I_D increases with V_{DS}
Saturation	$V_{GS} > V_{TH}$ and $V_{DS} \ge V_{GS} - V_{TH}$	$I_D = k(V_{GS} - V_{TH})^2$ (ideal square law)

Overdrive voltage

$$V_{ov} = V_{GS} - V_{TH}$$

Saturation current

$$I_D = k\left(V_{GS} - V_{TH}\right)^2$$

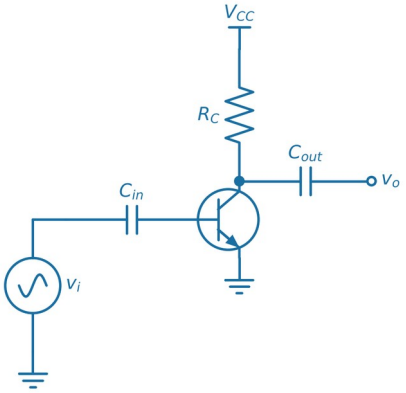
Applications

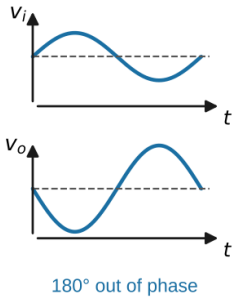
CMOS logic · switching · amplifiers · power control

7. BJT Amplifier Configurations

BJT amplifiers are classified by the terminal **common** to both input and output.

7.1 Common emitter (CE)

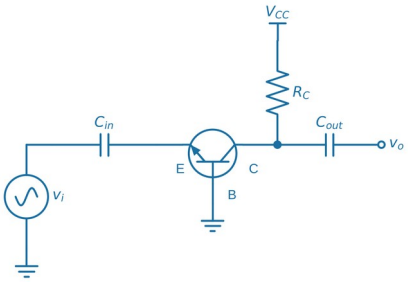


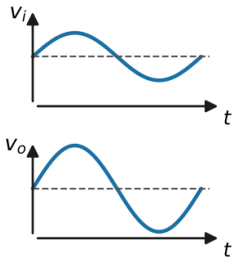


180° out of phase

- Input at base, output at collector; emitter AC-grounded.
- Voltage gain: high. Current gain: high.
- Input impedance: medium. Output impedance: high.
- Output is **180° out of phase** with the input.

7.2 Common base (CB)

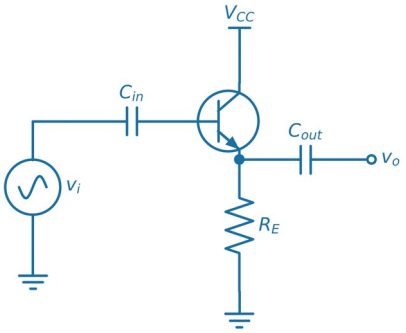


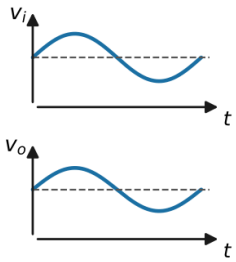


in phase

- Input at emitter, output at collector; base AC-grounded.
- Voltage gain: high. Current gain: less than 1.
- Input impedance: low. Output impedance: high.
- No phase reversal.

7.3 Common collector (CC) / emitter follower





in phase, $A_v < 1$

- Input at base, output at emitter; collector at V_{CC} (AC ground).
- Voltage gain ≈ 1 (slightly less). Current gain: high.
- Input impedance: high. Output impedance: low.
- No phase reversal.

7.4 Comparison

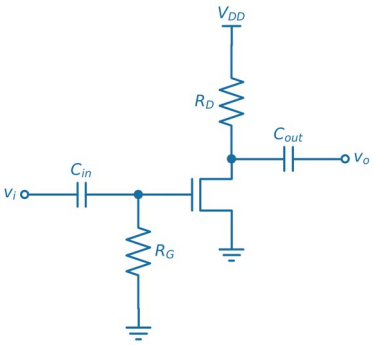
Parameter	Common emitter (CE)	Common base (CB)	Common collector (CC)
Voltage gain	High	High	≈ 1 (slightly less)
Current gain	High	Less than 1	High
Input impedance	Medium	Low	High
Output impedance	High	High	Low
Phase shift (v_o vs v_i)	180° (inverted)	0° (in phase)	0° (in phase)
Common use	General amplification	High-frequency stages	Buffer / impedance matching

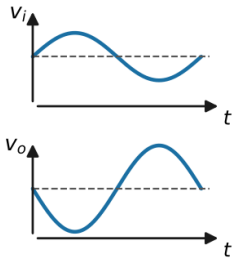
Table 2 — BJT amplifier configurations compared.

Most widely used
Common emitter — it is the only configuration with both high voltage gain and high current gain.

8. FET Amplifiers

8.1 Common source (CS)

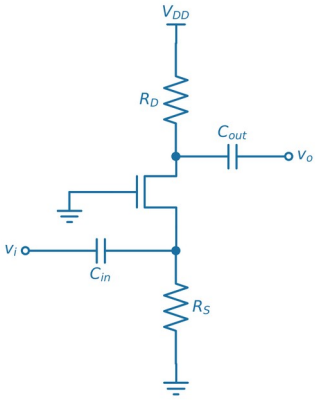


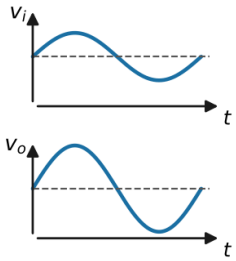


180° out of phase

- Source common (AC-grounded); input at gate, output at drain.
- High voltage gain: $A_v \approx -g_m(R_D \parallel R_L)$.
- Very high input impedance (≈ open circuit).
- Output is **180° out of phase** with the input.

8.2 Common gate (CG)

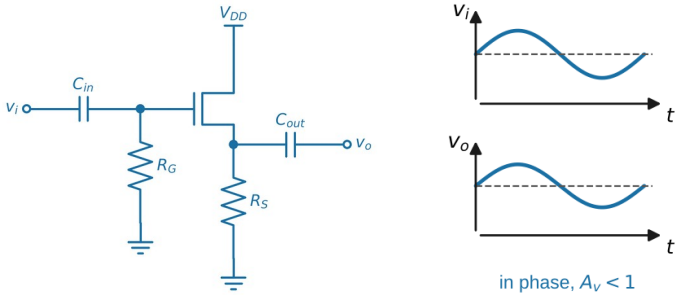




in phase

- Gate common (AC-grounded); input at source, output at drain.
- High voltage gain. Low input impedance: $R_{in} \approx 1/g_m$.
- High output impedance.
- No phase reversal.

8.3 Common drain (CD) / source follower



- Drain common (connected to V_{DD}); input at gate, output at source.
- Voltage gain slightly less than 1.
- Very high input impedance, low output impedance.
- No phase reversal.

8.4 Comparison of FET amplifier configurations

Parameter	Common source	Common gate	Common drain
Voltage gain A_v	High, ≈ $-g_m(R_D \parallel R_L)$	High	Slightly less than 1
Input impedance R_{in}	Very high (≈ ∞)	Low (≈ $1/g_m$)	Very high (≈ ∞)
Output impedance R_{out}	High	High	Low
Phase shift	180° (inverted)	0° (in phase)	0° (in phase)
Application	Voltage amplifier	High-frequency / current buffer	Impedance matching (buffer)

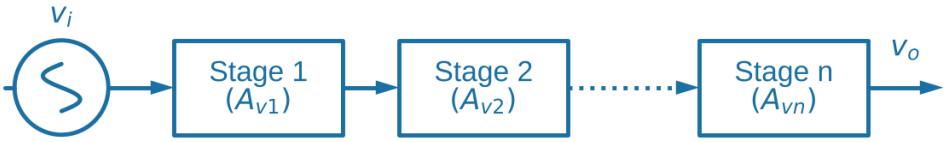
Table 3 — FET amplifier configurations compared.

> **Remember**
> FET configurations map onto BJT ones: **CS ↔ CE**, **CG ↔ CB**, **CD ↔ CC**.

9. Multistage & RC-Coupled Amplifiers

9.1 Why multistage?

- A single stage may not provide enough voltage gain.
- Cascading stages multiplies the gain (or adds it in dB).



$$A_{v(total)} = A_{v1} \times A_{v2} \times \cdots \times A_{vn}$$
$$Gain(dB) = A_{v1(dB)} + A_{v2(dB)} + \cdots + A_{vn(dB)}$$

9.2 RC-coupled amplifier

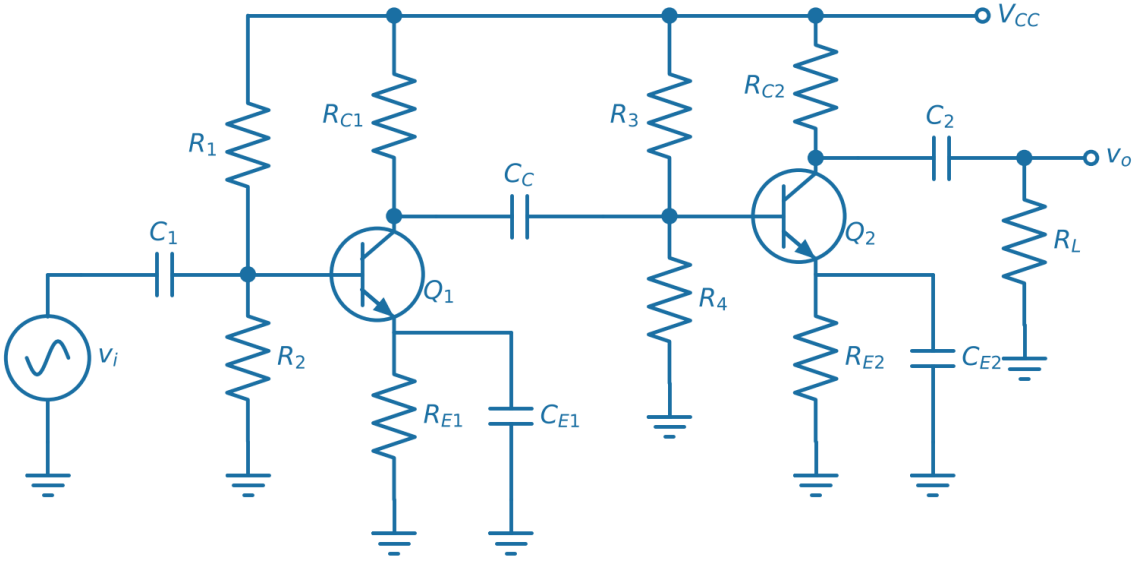


Figure 6 — Two-stage RC-coupled common-emitter amplifier.

Coupling capacitors (C_1, C_C, C_2) pass AC but block DC, so each stage keeps its own DC bias (operating point) independently. Emitter bypass capacitors C_{E1} and C_{E2} restore full AC gain.

9.3 Frequency response

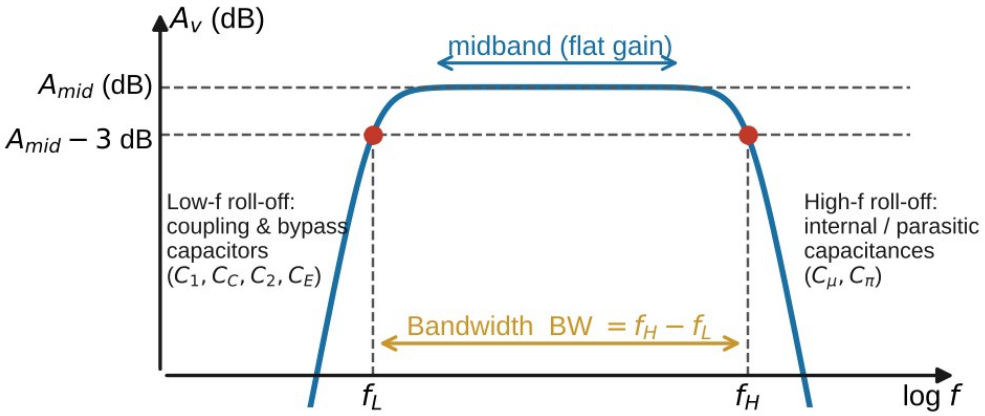


Figure 7 — Gain is flat across the midband and falls 3 dB at f_L and f_H; bandwidth BW = f_H − f_L.

9.4 Worked example

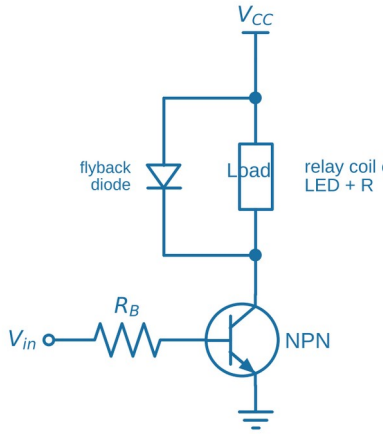
A two-stage amplifier has A_{v1} = 20 and A_{v2} = 30.

$$A_{v(total)} = 20 \times 30 = 600$$

$$A_{v(dB)} = 20 \log_{10}(600) \approx 55.6\,dB$$

10. Switching Circuits & Multivibrators

10.1 Transistor as a switch



Condition	Key values	Load status
OFF (cut-off)	$I_B = 0$, $I_C \approx 0$; $V_{CE} \approx V_{CC}$	Load OFF (no current)
ON (saturation)	I_B sufficient; $V_{CE(sat)} \approx 0.2$ V; I_C = load current	Load ON (current flows)

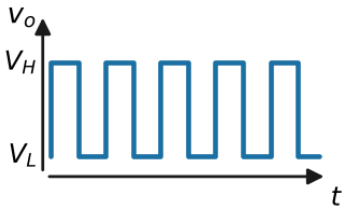
Base resistor selection

$$R_B = \frac{V_{in} - V_{BE}}{I_B} \quad I_B \geq \frac{I_C}{\beta_{min}}$$

$V_{BE} \approx 0.7$ V for silicon; in practice overdrive I_B by 2–5× to guarantee saturation

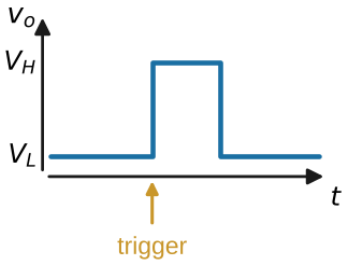
10.2 Multivibrators

(a) Astable



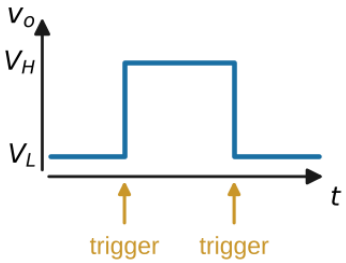
- **Astable:** no stable state.
- Free-running oscillator.
- Continuous square-wave output.

(b) Monostable



- **Monostable:** one stable state.
- One pulse per trigger (one-shot).
- Used as a timer / pulse generator.

(c) Bistable



- **Bistable:** two stable states.
- Changes state on each trigger.
- Used as a flip-flop / memory element.

10.3 Quick revision

JFET (Shockley)	MOSFET (saturation)	Amplifier gain	Negative feedback	Oscillation (Barkhausen)
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$I_D = k\left(V_{GS} - V_{TH}\right)^2$	$A_v = \frac{v_o}{v_i}$	$A_f = \frac{A}{1 + A\beta}$	$\lvert A\beta \rvert = 1$ *phase = 0° or 360°*

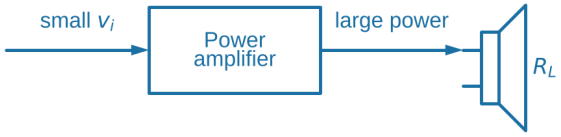
Common mistakes

- Never omit the **flyback diode** across a relay coil — the coil's back-EMF will destroy the transistor.
- Do not confuse **cut-off** (fully OFF) with **saturation** (fully ON).
- Check device polarity and connections: NPN vs PNP, diode direction, supply polarity.

11. Power Amplifiers

11.1 Purpose

- Power amplifiers deliver **large AC power** into a low-impedance load such as a speaker.
- They are judged by output power, efficiency, heat dissipation and distortion.



11.2 Amplifier classes

Class	Conduction angle θ	Q-point / biasing	Key features	Max. efficiency (ideal)	Typical use
A	360°	Q-point at middle of load line	Best linearity; low efficiency	25% (resistive load), 50% (transformer-coupled)	High-fidelity audio
B	180°	Biased at cut-off	Higher efficiency; crossover distortion	78.5% (theoretical)	Audio power amplifiers
AB	180° – 360°	Biased slightly above cut-off	Less crossover distortion than B; efficiency between A and B	Between 25% and 78.5%	Audio power amplifiers
C	< 180°	Biased well below cut-off	High efficiency; high distortion	High (can exceed 80%)	Tuned RF circuits

Table 4 — Power amplifier classes.

11.3 Input and output waveforms

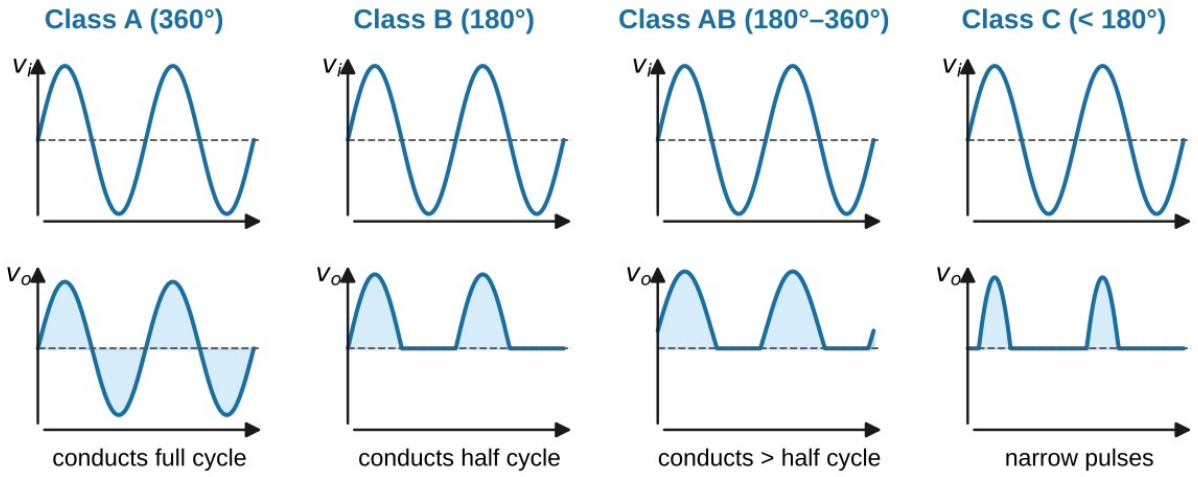
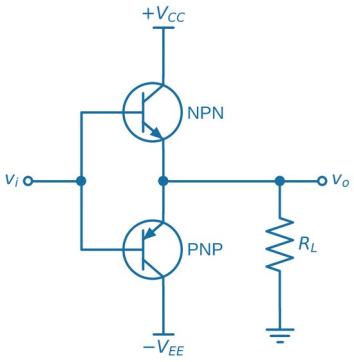


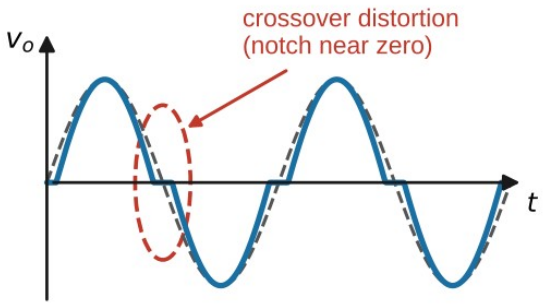
Figure 8 — Output conduction for classes A, B, AB and C.

11.4 Complementary push-pull class B



- **NPN** conducts the positive half-cycle ($v_o > 0$).
- **PNP** conducts the negative half-cycle ($v_o < 0$).
- Each transistor conducts for 180°, so efficiency approaches 78.5%.

11.5 Crossover distortion



Neither transistor conducts until $|v_i|$ exceeds about 0.7 V, causing a notch near zero. **Class AB** reduces it by giving both transistors a slight forward bias.

11.6 Important formulas

Power amplifier efficiency

$$\eta = \frac{P_{AC}}{P_{DC}} \times 100\,\%$$

P_{AC} = AC power delivered to the load; P_{DC} = DC power drawn from the supply

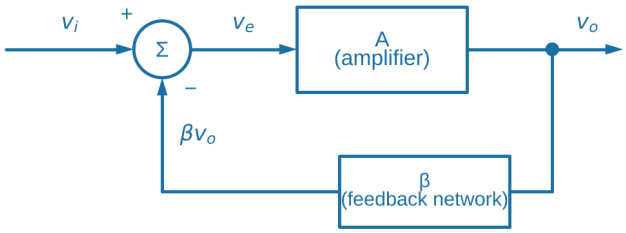
Load power (rms)

$$P_L = \frac{V_{L(rms)}^{\,2}}{R_L} = \frac{V_{L(peak)}^{\,2}}{2\,R_L}$$

12. Feedback & Oscillators

12.1 Feedback amplifier

- A fraction β of the output signal is fed back and combined with the input signal.
- Feedback can be **negative** (degenerative) or **positive** (regenerative).
- Used to obtain stable and predictable amplifier performance.



12.2 Negative feedback

$$A_f = \frac{A}{1 + A\beta}$$

- Gain decreases but becomes stable.
- Bandwidth increases.
- Distortion and noise decrease.
- Input and output impedances change depending on the topology (series / shunt).

12.3 Positive feedback

$$A_f = \frac{A}{1 - A\beta}$$

- Gain increases.
- If Aβ = 1 the system can sustain oscillations.
- Positive feedback supports oscillation.

12.4 Oscillator

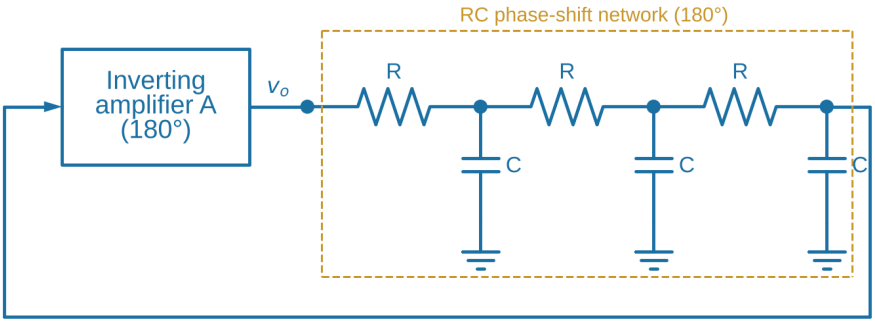
An oscillator converts **DC power into a periodic AC signal** without any external input signal.

12.5 Barkhausen criterion

$$|A\beta| = 1$$

and total phase shift $\angle A\beta = 0°$ or $360°$ at the oscillation frequency

12.6 RC phase-shift oscillator



- The inverting amplifier provides 180° of phase shift.
- Three RC sections provide another 180°.
- For equal R and C the amplifier needs |A| ≥ 29.

$$f_0 = \frac{1}{2\pi RC\sqrt{6}}$$

12.7 Common oscillator types

Oscillator type	Typical frequency range	Feedback network / key features	Frequency
RC phase shift	Audio / low frequency	Three RC sections (phase-shift network); |A| ≥ 29	$f_0 = \frac{1}{2\pi RC\sqrt{6}}$
Wien bridge	Low-distortion sine wave	RC lead-lag bridge; amplifier gain of 3 (for equal R, C)	$f_0 = \frac{1}{2\pi RC}$
Hartley	Radio frequency	Two inductors in series (tapped) + one capacitor	$f_0 = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$
Colpitts	Radio frequency	One inductor + two capacitors (capacitive divider)	$f_0 = \frac{1}{2\pi\sqrt{L\frac{C_1C_2}{C_1+C_2}}}$

Table 5 — Common oscillator types. Hartley frequency ignores mutual inductance between L_1 and L_2.

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